Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **OUT1**
2. **–IN1**
3. **+IN1**
4. **–VS**
5. **+IN2**
6. **–IN2**
7. **OUT2**
8. **+VS**

**.045”**

**.065”**

**8**

**7**

**6**

**5**

**1**

**2**

**3**

**4**

**ADI95**

**8042**

**MASK**

**REF**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: +VS**

**Mask Ref: 8042**

**APPROVED BY: DK DIE SIZE .045” X .065” DATE: 1/4/23**

**MFG: ANALOG DEVICES THICKNESS .019” P/N: AD8042A**

**DG 10.1.2**

#### Rev B, 7/19/02